AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 18, line 1, with the following rewritten paragraph:

Referring to **FIGURE 6**, a schematic block diagram shows a register file **600** for a VLIW processor **100** that includes global and local register partitioning. The Very Long Instruction Word (VLIW) processor has a plurality of functional units including three media functional units **622**, **624**, and **626**, and a general functional unit **620**. The processor **100** also includes a multi-ported register file **600** that is divided into a plurality of separate register file segments **610**, **612**, **614**, and **616**, each of the register file segments being associated to one of the plurality of functional units and to a decoder block of decoder **602**. The register file segments **610**, **612**, **614**, and **616** are partitioned into local registers and global registers. The global registers are read and written by all functional units **620**, **622**, **624**, and **626**. The local registers are read and written only by a functional unit associated with a particular register file segment. The local registers and global registers are addressed using register addresses in an address space that is separately defined for a register file segment/functional unit pair including register file segment **610**/general functional unit **620**, register file segment **612**/ media functional unit **622**, register file segment **614**/ media functional unit **624**, and register file segment **616**/ media functional unit **626**.